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JACOB, MARY C	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/729,701	WEI ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,23,26-28,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,23,26-28,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The response filed 1/10/07 has been received and considered. Claims 1-12, 23, 26-28, 31 and 32 have been presented for examination.

Drawings

2. The objections to the drawings recited in the Office Action dated 11/17/06 are withdrawn in response to the amendments to the specification.

Specification

3. The objections to the specification recited in the Office Action dated 11/17/06 are withdrawn in response to the amendments to the specification.

Claim Objections

4. The claim objections, recited in the Office Action dated 11/17/06 and not repeated below, have been withdrawn in response to the amendments to the claims.

5. Claims 1, 7, 23 and 28 recite "identifying...circuit elements". It is noted that there is no limitation stating what kinds of circuit elements are identified or how the circuit elements are identified. This limitation, therefore, can be interpreted broadly.

6. Claims 23 and 28, step f "initial minimum and maximum values" should read, "initial minimum and initial maximum values".

7. Claims 24 and 28 recite, "a current value of the parameter under characterization that is half..." in steps (i) and (k). Because there are so many recitations of "current

value" in the claims, it would be better if this "value" were given a different name to avoid confusion with the "current minimum" and "current maximum" values.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. The claim rejections under 35 U.S.C. 112, second paragraph, recited in the Office Action dated 11/17/06 and not repeated below, have been withdrawn in response to the amendments to the claims.

10. Claims 1-12, 23, 26-28, 31 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claims 1 and 23 recite, "identifying, with a computer processor, circuit elements of the memory circuit design". It is unclear how a computer processor can "identify" something. It is understood that the computer processor may execute instructions wherein the instructions can "identify" something, but the processor itself, cannot.

12. Claims 7 and 28 recite, "a computer including a computer program configured to cause at least one processor to execute the following instructions". This limitation is unclear since it is not understood how the computer can include a computer program. A computer can include some storage device, such as a memory, that stores a computer program, however, the claims fail to recite this storage element. Further, it is unclear whether the limitation is intended to infer that the "computer" is "configured to cause at

least one processor to execute the following instructions" or whether the "computer program" is "configured to cause at least one processor to execute the following instructions".

13. Claims 9-11 recite limitations such as "cause the processor" to measure, compare and identify. It is unclear how a "processor" can measure, compare and identify anything. It is understood that a computer processor may execute instructions wherein the instructions can "identify", "measure" or compare" something, but the processor itself, cannot.

14. Claims 23 and 28, steps h-l contain various recitations of "the parameter" that is not followed by "under characterization", for example, step h, lines 1 and 2. Therefore, it is unclear whether "the parameter" is referring to "a minimum circuit parameter" or "a criterion parameter". It is therefore also unclear where step l recites "repeating steps l-k until the criterion parameter converges", how these steps are directed to the "criterion parameter" and not the ""minimum circuit parameter" being "characterized".

15. Claims 23 and 28, step h recites, "setting current maximum and minimum values of the parameter to the initial maximum and minimum values of the parameter". This language is confusing because it appears that the "current" values in step h are the same values as the "initial" values because there is no recitation in steps a-g of different maximum and minimum values of the parameter being calculated. Therefore, this step appears to be unnecessary.

16. Claims 23 and 28, step (j) recites, "simulating the critical path netlist with the current maximum and minimum values of the parameter". As discussed above with

reference to step h, it appears that the "current" values are the same values as the "initial" values. Therefore, this simulating step appears to be repetitive since the simulating with these values has already been done. The claim language is also confusing in that it recites "simulating...with the current minimum and maximum values" which indicates one simulation, and then "determining" "whether both simulations..." which indicates more than one simulation is run.

17. Claims 23 and 28, step (k) further recites the "current minimum" and "current maximum" values, however, for the same reasons as set forth for step (h), it is unclear whether these "current" values are different from the "initial" values since there is no recitation of new values being calculated.

18. Claims 26, 27, 31 and 32 recite "wherein the simulation". However, there are various recitations of simulations performed in Claims 23 and 28, therefore, it is unclear what "simulation" these claims refer to.

19. Due to the number of 35 U.S.C. 112, second paragraph rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejection(s), however, the list of rejections may not be inclusive. Applicant should refer to these rejections as examples of deficiencies and should make all necessary corrections to eliminate the 35 U.S.C. 112, second paragraph problems and place the claims in proper format.

Due to the vagueness and a lack of a clear definition of the terminology and phrases used in the specification and claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 101

20. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

21. Claims 1-12, 23, 26-28, 31 and 32 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are a recitation of abstract ideas and fail to produce a concrete, useful or tangible result. For example, Claims 1 and 7 recite the result, "comparing the maximum voltage difference between bit lines to a noise margin to verify the signal strength of the bit lines", however, this is a recitation of an abstract idea and even though the signal strength of the bit lines is "verified", there is no recitation of a concrete, useful or tangible result since there is no "real world" output of a result. Claims 23 and 28 recite the results, "ceasing simulation if both simulations indicate a failed status" or "repeating steps I-k until the criterion parameter converges to a prescribed bisection". These "results" fail to produce any "real-world" result as the ceasing of simulations and the criterion parameter appear to remain embodied within the computer environment.

22. The addition of "computer implemented" and "computer processor" to Claim 1 does not remedy the need for a concrete, useful or tangible result as the "verification" still appears to be embodied within the computer.

23. The addition of "including computer program" configured to cause at least one processor" in Claim 7 further leads to the analysis that the "computer program" is not combined with a computer readable medium and therefore, this limitation is directed to software per se which is non-statutory subject matter. It is further noted that the specification (page 5, lines 3-7), recites that "a computer readable medium" can be a "propagation medium" along with some examples of this "propagation medium" which implies the computer readable medium can be a "signal" and therefore, encompasses a computer readable medium that is non-statutory since "signals" fail to fall within one of the four classes of statutory subject matter.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

25. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuan et al (US Patent 6,249,901) in view of Laurent ("Sense Amplifier Signal Margins and Process Sensitivities", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Volume 49, No. 3, March 2002).

26. As to Claims 1 and 7, Yuan et al Teaches a computer implemented method of simulating a memory circuit design to verify timing characteristics, the method comprising: identifying, with a computer processor, circuit elements of a memory circuit design (Figure 5, elements 204, 208, 210; column 9, lines 35-39, lines 65-67), extracting a least one critical path circuit from the circuit elements (Figure 5, elements 240 and 242; column 9, line 67-column 10, line 2; column 10, lines 45-52; Figure 8; column 19, lines 23-28) simulating the critical path circuit (column 6, lines 40-56), measuring a circuit parameter and comparing the measured circuit parameter to a prescribed value to verify that the circuit parameter is within an acceptable value (column 21, lines 17-51) in an optimization process for optimizing timing parameters (column 19, lines 15-23).

27. Yuan et al does not expressly teach: the measured circuit parameter in the optimization process being a maximum voltage difference between bit lines and the maximum voltage difference between bit lines being compared to a noise margin.

28. Laurent teaches that during the sensing operation in DRAMs, a voltage differential on a pair of bit lines is amplified by a sense amplifier to rail voltages which can then be used to restore original data in the DRAM memory cells and to drive the read buffers, however, to perform this operation successfully, the sensing system must be capable of distinguishing between two charge states and is commonly characterized by specifying its signal margins (Introduction, paragraph 1, lines 1-18). Therefore, Laurent teaches a method for determining the signal margins of a sense amplifier (Abstract) wherein the method includes simulating a sense amplifier system wherein a voltage difference is varied between bit lines (Figure 2, section II, paragraph 2, lines 1-7) and wherein the maximum voltage difference between the bit lines is used to determine a noise margin (Figure 2, section II, paragraph 2, lines 7-13; section II, paragraph 4, lines 1-3, paragraph 5, lines 1-2).

29. Yuan et al and Laurent are analogous art since they are both directed to the simulation of a memory circuit and the characterization of the memory circuit parameters.

30. Since Laurent teaches that in order to restore the original data in DRAM memory cells and to drive the read buffer, the sensing system must be capable of distinguishing between two charged states and is commonly characterized by specifying its signal margins (Introduction, paragraph 1, lines 1-18), and further teaches varying the voltage differential between bit lines to determine the signal margins of the sensing system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the simulation of a memory circuit for the characterization of memory

circuit parameters as taught in Yuan et al to include the characterization of the maximum voltage difference between bit lines by measuring the voltage difference and comparing it to a noise margin since one of ordinary skill in the art would know that it would be necessary to determine the voltage differentials on the bit lines that would allow for proper operation of the sensing system in the memory circuit, wherein the voltage differential must fall within the predetermined noise margin of the sense amplifier circuit to ensure proper operation.

31. Claims 2-6, 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuan et al in view of Laurent as applied to claims 1 and 7 above, and further in view of Sandhu (US Patent 5,521,874).

32. Yuan et al in view of Laurent teach (claims 1 and 7) simulating a memory circuit design in order to verify the signal strength of bitlines, (claims 4 and 10) measuring the voltage difference between bit lines at a sensing time (Figure 2), and (claims 5 and 11) comparing the voltage difference between bit lines to a noise margin at the sensing time to verify the signal strength of the bit lines (section II, paragraphs 3-5).

33. Yuan et al in view of Laurent do not expressly teach (claims 2, 6, 8 and 12) wherein the voltage difference between bit lines is the voltage difference between bit and bitb lines and (claims 3 and 9) identifying sense amplifier enable node after extracting the critical path circuit.

34. Sandhu teaches a novel differential to single ended sense amplifier that utilizes a minimum number of stages to convert a differential input signal received from complementary bit lines to a single ended output signal indicative of the state of the

data stored in a selected memory cell connected to the complementary bit lines wherein the circuit is constructed to operate with low voltage swings thereby increasing the switching speed and the sense speed (column 2, line 65-column 3, line 6). Sandhu teaches complementary bitlines, bit and bitb, that apply complementary signals to the input of a differential sense amplifier (column 1, lines 45-53) and a sense amplifier enable node that enables or disables the current sources in the circuit stages, thereby powering down the sense amplifier (column 5, lines 3-14).

35. Yuan et al in view of Laurent and Sandhu et al are analogous art since they are both directed to the design of a memory circuit that includes sense amplifiers.

36. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the simulating of a memory circuit design to verify the signal strength of bitlines as taught in Yuan et al in view of Laurent to further include the measurement of the voltage differential to be between the bit and bitb lines and by identifying the sense amplifier enable node since Sandhu teaches a novel differential to single ended sense amplifier that utilizes a minimum number of stages to convert a differential input signal received from complementary bit lines to a single ended output signal indicative of the state of the data stored in a selected memory cell connected to the complementary bit lines wherein the circuit is constructed to operate with low voltage swings thereby increasing the switching speed and this the sense speed (column 2, line 65-column 3, line 6) and further teaches that the inputs to a differential sense amplifier are the bit and bitb lines (column 1, lines 45-53) and that the sense amplifier enable signal enables the sense amplifier to operate (column 5, lines 3-14).

37. Claims 23-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuan et al in view of Laurent.

38. As to Claims 23 and 28, Yuan et al teaches: (a) identifying with a computer processor, circuit elements to be characterized (Figure 5, elements 204, 208, 210; column 9, lines 35-39, lines 65-67); (b) extracting a critical path netlist from the circuit elements (Figure 5, elements 240 and 242; column 9, line 67-column 10, line 2; column 10, lines 45-52; Figure 8; column 19, lines 23-28); (c) simulating the critical path netlist with a maximum initial value of the parameter under characterization (column 10, lines 50-52; Figure 11A, element 558); (d) simulating the critical path netlist with a minimum initial value of the parameter under characterization (Figure 11A, element 562; column 21, lines 35-38; column 20, lines 19-22); (e) calculating a criterion parameter (column 20, element 16-42; Figure 11A, elements 556, 558, 562; column 21, lines 17-21); (f) determining whether both the simulations based on the initial minimum and maximum values of the parameter under characterization indicate a success or failed status (Figure 11A, element 566; column 21, element 52-56); and (g) ceasing simulation if both simulations indicate a success or failed status (column 20, lines 33-47); otherwise,

(h) setting current maximum and minimum values of the parameter to the initial maximum and minimum values of the parameter, respectively (Figure 11A, steps 554);

(i) determining a current value of the parameter under characterization that is half the sum of the current maximum and minimum values of the parameter (column 22, equation 2);

(j) simulating the critical path netlist with the current maximum and minimum values of the parameter and determining whether the simulation indicates a success or failed status (Figure 11A, elements 568-556; Figure 11B, elements 592, 594, 596);

(k) setting the current value of the parameter to the current minimum value of the parameter if both simulations based on the current maximum and minimum values of the parameter indicate a success or failure status (Figure 11B, elements 596 and 598); or setting the current value of the parameter to the current maximum value of the parameter otherwise (Figure 11B, elements 600-602); and

(l) repeating steps (i)-(k) until the criterion parameter converges to a prescribed bisection (Figures 11A-11B, steps 570-576)

39. As to Claims 26 and 31, Yuan et al teaches: wherein the simulation indicates a failed status if a data output error of the simulation is above a prescribed threshold (column 20, lines 16-42; column 21, lines 29-51).

40. As to Claims 27 and 32, Yuan et al teaches: wherein the simulation indicates a failed status if the measured parameter is above a prescribed value (column 21, lines 28-51).

41. Yuan et al does not expressly teach: (claims 23 and 28) characterizing a circuit parameter sensitive to a noise disturbance against a prescribed noise margin in a circuit design, the simulation determining against a prescribed noise margin whether both the simulations indicate a failed status, (claims 27 and 32) wherein the simulation indicated a failed status if the measured noise is above a prescribed noise margin.

42. Laurent teaches that during the sensing operation in DRAMs, a voltage differential on a pair of bit lines is amplified by a sense amplifier to rail voltages which can then be used to restore original data in the DRAM memory cells and to drive the read buffers, however, to perform this operation successfully, the sensing system must be capable of distinguishing between two charge states and is commonly characterized by specifying its signal margins (Introduction, paragraph 1, lines 1-18). Therefore, Laurent teaches a method for determining the signal margins of a sense amplifier (Abstract) wherein the method includes simulating a sense amplifier system wherein a voltage difference is varied between bit lines (Figure 2, section II, paragraph 2, lines 1-7) and wherein the maximum voltage difference between the bit lines is used to determine a noise margin (Figure 2, section II, paragraph 2, lines 7-13; section II, paragraph 4, lines 1-3, paragraph 5, lines 1-2).

43. Yuan et al and Laurent are analogous art since they are both directed to the simulation of a memory circuit and the characterization of the memory circuit parameters.

44. Since Laurent teaches that in order to restore the original data in DRAM memory cells and to drive the read buffer, the sensing system must be capable of distinguishing

between two charged states and is commonly characterized by specifying its signal margins (Introduction, paragraph 1, lines 1-18), and further teaches varying the voltage differential between bit lines to determine the signal margins of the sensing system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the simulation of a memory circuit for the characterization of memory circuit parameters as taught in Yuan et al to include the characterization of a maximum and minimum value for a parameter and determining against a prescribed noise margin, whether the parameters fall within the noise margin of a device and indicating this with a success or failed status in a simulation, since it is understood that a circuit, such as a sense amplifier in a memory circuit, requires the input voltages to fall within the prescribed noise margin of the circuit in order for the circuit to operate properly.

Response to Arguments

45. Applicant's arguments filed 1/10/07 have been fully considered but they are not persuasive.

46. Applicant argues: "The Laurent paper has little to do with the presently claimed invention" and "...even thought the Laurent paper discloses the steps of applying known voltage differential and amplifying the voltage differential to check if voltage of bit lines are near VDD and VSS, it fails to teach the step of measuring the maximum voltage difference between bit lines in the sense of the present application. Perhaps, more importantly, the Laurent reference is silent as to the prescribed noise margin, much less

the step of comparing the maximum voltage difference between bit lines to a prescribed noise margin" (pages 14-15).

47. As to this argument, it is understood from the claim language that the present invention is directed to a method of characterizing the parameters of a memory circuit design as is Laurent, therefore, they are determined to be analogous art. Further, although Laurent does not expressly teach measuring the maximum voltage difference between bit lines, it is noted that the voltage differential is applied to the bit lines and further varied from large positive values to large negative values and the cell response was studied for each variation (as shown in Figure 2, and discussed in section II, paragraph 2, lines 1-13). Therefore, it is understood that in this application, the voltage differential being "varied" between the bit lines is analogous to "measuring" the voltage difference between the bit lines since the same result, that is, the voltage difference between the bit lines, is known. As to comparing the maximum voltage difference between the bit lines to a prescribed noise margin to verify the strength of the bit lines, it is understood and taught by the teachings of Laurent that there are particular voltage differentials between the bit lines that allow for the proper operation of the sense amplifier, that is, the voltage differential, falling within the signal margins of the sense amplifier, will allow for the proper operation of the sensing circuit. Therefore, it would be obvious to one of ordinary skill in the art when characterizing what parameters would allow for proper operation of a memory circuit, to determine a maximum voltage difference between the bit lines that would fall within a pre-determined noise margin of the sense amplifier circuit.

48. Applicant argues, "The combination of teachings in the Laurent paper and Yuan et al is not obvious", "It is not clear how the steps of the Laurent paper for finding signal margins can be performed in the Yuan et al system so as to verify the signal strength of bit lines. Nor would it be logical to modify the method steps of the Laurent paper to further include steps of identifying circuit elements of the memory circuit and extracting a memory circuit path insofar as the Laurent method steps are performed on a given system and as a consequence, these two steps are not needed to determine the two signal margins" (pages 15-16).

49. As to this argument, both Yuan et al and Laurent are directed to the characterization of circuit parameters for a memory circuit through simulation; therefore, they are determined to be analogous art. It would also be obvious to one of ordinary skill in the art to use the memory characterization system as taught in Yuan et al to characterize and optimize other memory design parameters, such as a maximum voltage differential of bit lines that would fall within the noise margins for the memory circuit to perform properly in order to determine design parameters that would allow wanted circuit functionality.

Conclusion

50. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

51. Wendell (US Patent 5,920,517) teaches a memory array test and characterization capability is disclosed which allows DC characterization of the memory cells, the bit lines, and the sense amplifiers.

52. Kang et al, ("A Deep Sub-Micron SRAM Cell Design and Analysis Methodology, Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems, 2001) teaches a comprehensive SRAM design and diagnosis methodology including optimization paradigms on cell stability test against power supply fluctuations, SRAM access time, bit line voltage switching and static noise margin analysis.

53. Lee et al ("Static Noise Margin and Soft-Error Rate Simulations for Thin Film Transistor Cell Stability in a 4Mbit SRAM Design", IEEE International Symposium on Circuits and Systems, 1995) teaches evaluating the static and dynamic stabilities of a bit cell in an SRAM design by SNM and SER HSPICE simulations.

54. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/22/07

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

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Mary C. Jacob
Examiner
AU2123

MCJ
3/20/07